ABSTRACT OF THE DISCLOSURE

At the same when the control signal line of a printer controller is connected to the input terminal of a three-state buffer, the control signal line is connected also to the D input terminal of the flip-flop that operates according to the FFCK clock. The control signal of Q output signal of the flip-flop is inputted into the AND gate circuit, and the output signal of the gate is inputted into the control terminal of three-state buffer. Accordingly, by synchronizing the signal to the place where the level of control signal line starts, the level of data signal line changes from level 1 to the level of output. After that, waveform rounding that is generated at the time of releasing the signal line is reduced to enable higher communication speed.